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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,268	04/01/2004	Takashi Manabe	Q80846	8109

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EXAMINER	
ABDULSELAM, ABBAS I	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,268	MANABE, TAKASHI	
	Examiner	Art Unit	
	Abbas I. Abdulselam	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2 and 13-14 rejected under 35 U.S.C. 102(e) as being anticipated by Iwanari (USPN 6865101).

Regarding claim 1, Iwanari (USPN 6865101) teaches a memory circuit comprising *(Fig. 6, memory system, col. 10, lines 54-56)*: a memory *(Fig. 6 (10, 11));* a delay circuit *(Fig. 6 (13), Fig. 9 (13b))* for generating a delay clock signal by delaying a reference clock signal *(col. 11, lines 33-41, col. 12, lines 20-21, see delay time in Fig. 7)*; at least one detection circuit *(Fig. 6 (22, 24))* for detecting a temperature of the memory or therearound *(col. 11, lines 4-6, Fig. 6 (22))*, and/or a power-supply voltage of the memory or therearound *(col. 11, lines 1-4, Fig. 6 (24, 26))*; and a control circuit for generating a control signal according to the temperature *(col. 11, lines 7-11, Fig. 6 (22, 23))* or the power-supply voltage detected by the detection circuit (*col. 11, lines 11-19, Fig. 6 (24, 25))*, wherein a delay amount of the delay clock signal is controlled by the

control signal *(col. 11, lines 44-65, col. 12, lines 1-5, Fig. 6 (11, 14, 23, 24)).*

Regarding claim 13, Iwanari teaches a method for operating a memory circuit including *(Fig. 6, memory system col. 10, lines 54-56)* a memory *(Fig. 6 (10, 11))*, the method comprising the steps of: generating a delay clock signal *(Fig. 6 (13), Fig. 9 (13b))* by delaying a reference clock signal *(col. 11, lines 33-41, col. 12, lines 20-21, see delay time in Fig. 7)*; detecting *(Fig. 6 (22, 24))* a temperature and/or a power-supply voltage of the memory *(col. 11, lines 4-6, Fig. 6 (22), col. 11, lines 1-4, Fig. 6 (24, 26))*; and determining a delay amount of the delay clock signal according to the detected temperature and/or the detected power-supply voltage*(col. 11, lines 44-65, col. 12, lines 1-5, Fig. 6 (11, 14, 23, 24)).*

Regarding claim 14, Iwanari teaches a method for operating a memory circuit *(Fig. 6 (10, 14), col. 10, lines 54-56)* including a memory *(Fig. 6 (10, 11))*, a first clock, and a second clock *(col. 11, lines 33-41, col. 12, lines 20-21, see vertical time axis Fig. 7)*; the method comprising the steps of: driving the memory in synchronization with the first clock *(col. 11, lines 24-30, note that synchronization with respect to memory (10), and "time required is inherent");* capturing data read from the memory and/or data written into the memory in synchronization with the second clock *(col. 11, lines 24-35, col. 12, lines 11-13, note that synchronization corresponding to different timing is inherent)* detecting a temperature and/or a power-

supply voltage of the memory or therearound *(col. 11, lines 1-6, Fig. 6 (22, 24, 26))*; and controlling a relative delay amount between the first clock and the second clock according to the detected temperature and/or the detected power-supply voltage *(col. 11, lines 44-65, col. 12, lines 1-5, Fig. 6 (11, 14, 23, 24))*.

Regarding claim 2, Iwanari teaches a data capture circuit *(Fig. 6 (9))* for capturing data read from the memory and/or data written into the memory, wherein the memory and/or the data capture circuit operates in synchronization with the delay clock signal *(col. 11, lines 24-35, col. 12, lines 11-13, Fig. (7-8), col. 12, lines 45-59)*.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwanari (USPN 6865101).

Regarding claim 3-4, Iwanari teaches as shown in Fig. 2 selector switches (13a), delay circuits (13b), such that each of the selector switches

13a is provided between two delay circuits 13b, and a code circuit 13c that controls a plurality of selector switches 13a (three switches in the case of the figure) is arranged in the timing generating circuit 13 (col. 7, lines 53-67).

Iwanari does not specifically teach a delay circuit being formed as a PLL circuit or a DLL circuit.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize Iwanari's delay circuit (13b) along with selector switches (13a) as configured in Fig. 2 for the purpose of outputting a control signal (12) coming out of timing generation circuit (13) (shown in Fig. 1), as taught by Iwanari (col. 8, lines 4-10).

5. Claims 5-8 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwanari (USPN 6865101).

Regarding claims 5-8, and 9-12, Iwanari does not specifically teach image data output from the memory circuit is displayed, wherein the image data output from the memory circuit is displayed by the plasma display panel.

Suzuki et al. (USPN 6415057) on the other hand teach as shown in Fig. 6 an encoded information, outputted at the output terminal 18, is

recorded on a semiconductor memory, decoded to picture signals, which are directly sent to a variety of display apparatus, including plasma display (100) (see Fig 13) (col. 9, lines 7-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Iwanari's memory system shown in Fig. 6 to be utilized with respect to Susuki's plasma display (100) as shown in Fig. 13, because plasma display along with other types is compatible with a variety of recoding mediums including a semiconductor memory as taught by Susuki (col. 9, lines 7-17).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following arts are cited for further reference.

U.S. Pat. No. 7,113,153 to Kubota et al.

U.S. Pat. No. 7,038,648 to Yamakawa et al.

U.S. Pat. No. 6,598,139 to Kawaguchi et al.

U.S. Pat. No. 5,744,909 to Amano

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is 571-272-7685. The examiner can normally be reached on Monday through Friday from 9:00A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abbas I Abdulselam
Examiner
Art Unit 2629
June 18, 2007